Abstract—This paper presents an electro-thermal model of an Insulated Gate Bipolar Transistor (IGBT) switch suitable for the simulation of switching and conduction losses in a large class of Voltage Sourced Converter (VSC) based FACTS devices. The model is obtained by mathematical derivation of loss equations from the known sub-microsecond device switching characteristics, and through the selection of appropriate differential equation parameters for representing the thermal performance. The model is useful in determining the device’s heat generation, its junction temperature as well the cooling performance of the connected heat sinks. The model provides accurate results without recourse to an unreasonably small time-step.

Index Terms—IGBT, switching losses, thermal performance, electromagnetic transient simulation, voltage-sourced converter

I. INTRODUCTION

The insulated gate bipolar transistor (IGBT) is widely used in many modern power-electronic applications in power transmission and distribution systems. Estimation of power loss and junction temperature of power semiconductor devices has become a major issue with the growth of high switching frequency applications such as pulse width modulated (PWM) inverters, where switching losses constitute a significant portion of the power dissipation in the semiconductor device. Power electronic system manufacturers can utilize the relatively low but significant thermal capacity of the power semiconductors to obtain short duration overloading well in excess of continuous ratings [1]. Tools for accurate prediction of device power dissipation and junction temperature become important in achieving optimized solutions in terms of performance, thermal management and packaging.

Most electromagnetic transient programs (emtp-type) model power electronic devices as on-off switches or two state resistances [2]. This simple representation is sufficiently accurate to simulate the system-level electrical behaviour of power electronic circuits [3]. However, the determination of switching and conduction losses requires the consideration of the physics of the switching process, which lasts only about several hundreds of nanoseconds. To model this process in detail would require a very small time-step which would result in an unacceptably large CPU time when simulating large multi-device power electronic systems (such as FACTS devices).

Previous efforts to address the issue of accurate estimation of power losses include using specially defined switching functions obtained through measurements [5] or the use of lookup tables or fitted curves to define power losses as a function of voltage, current and junction temperature [4],[6],[7]. The first method requires very small time steps, whereas the second is approximate.

Another approach that has been proposed is the use of simple functions derived for losses based on the typical switching waveforms [8],[9],[10]. The method presented in this paper extends the above approach by ‘filling-in’ the device’s current and voltage waveforms in between the simulation time step to conform to the physics of the switching process. With these estimated waveforms it becomes possible to calculate the losses.

Once the losses are estimated, it becomes necessary to solve the heat-flow problem in order to determine temperatures and cooling requirements. The most accurate method for doing so is through three dimensional finite-element based modeling [11], which is again impractical in system level simulations. The more acceptable and commonly used approach is to model the thermal behaviour by using equivalent network of thermal resistances and capacitances [1],[12],[13].

This paper describes a complete electro-thermal model of IGBT and parameter extraction method. Effort has made to obtain most model parameters from the published data sheets. The dependency of the switching losses on various factors such as switching voltage, switching current, reverse recovery of freewheeling diode, stray inductance and capacitance are taken into account. The model was implemented in PSCAD/EMTDC™, a well known emtp-type program.

Validation of the model was conducted using a simple laboratory set-up and by comparison with published loss curves by the manufacturer. The paper concludes with an application example for loss determination in a PWM inverter.

II. DEVELOPMENT OF A SUITABLE SWITCH MODEL FOR EMTP-TYPE PROGRAMS

A. Method for Interfacing

The majority of emtp-type programs are used for large system studies, and therefore usually employ simple on/off type representations for devices such as diodes, thyristors, GTOs and IGBTs. For such studies, a detailed representation of the physics of the switching device, which requires time-
steps in order of several nanoseconds, would be over time consuming.

The switching loss model developed in this paper is applicable to IGBT devices subject to ‘hard switching’ which are widely used in today’s FACTS devices. Each switch consists of an IGBT in anti-parallel with a freewheeling diode. The turn-on of the IGBTs (and hence the turn-on switching loss) is significantly affected by the reverse recovery behaviour of the freewheeling diode and the parasitic inductances. Although the discussion below is specific to hard-switched IGBTs, as shown in the test circuit of Fig. 2, the proposed concepts are readily extendable to other device types.

![Diagram](image)

**Fig. 1. Interface between the electro-thermal device model and the network model**

The approach presented in this paper and depicted schematically in Fig.1, adds an additional layer to this simple device model which only makes minor dynamic updates to the parameters within the host emtp program. The losses in the device are estimated by observation of the pre- and post-switching currents and voltages using the algorithm described below. These losses become the inputs to a dynamic model of the heat management system (thermal path) which computes the temperature changes in various parts of the system. Because the device losses are functions of temperature, the computed device temperature is then used to change the parameters of the switch loss model for the next time-step.

### B. Modelling of Device Losses

The losses in a power-switching device can be classified as conduction losses, turn-on switching losses, turn-off switching losses and off-state blocking losses. The conduction loss is calculated in a straightforward manner as the product of the device current and the forward saturation voltage; and the blocking loss is the product of the blocking voltage and the leakage current.

However, the determination of switching losses is a challenge because the duration of the switching process is in the order of a few hundred nanoseconds. The emtp-type program typically uses a much larger time-step (tens of microseconds) in order to achieve a reasonable CPU time for simulating the entire network. This paper proposes a workaround to this apparently impossible situation by developing algebraic equations that represent the voltage and current waveforms during the switching event based on the fact that the current and voltage waveforms during switching are principally a function of the pre- and post- switching voltage and current. These equations ‘fill-in’ the intermediate sub-microsecond values of voltage and current in between the larger sampling instants dictated by the emtp time-step of several microseconds. The parameters of these equations are derivable from the pre- and post-switching voltages, currents and other physical data. The energy loss can then be calculated analytically (not numerically!) by integrating the product of developed voltage and current equations resulting in a formula for the switching loss. Thus the emtp-type simulation can be conducted with a larger time-step, with the developed formula providing an estimate of the loss at each switching.

1) Diode Turnoff Loss Formula

As mentioned above, the IGBT turn-on losses are affected by the reverse recovery performance of the diode, which is now discussed. The turn-off waveforms of a diode are shown in Fig. 3. As the diode current falls, part of its stored charge is removed due to recombination. The amount of the charge removed is a function of the rate of current change $dI_d/dt$. This rate is determined by the turn-on speed of the IGBT in the opposite leg. The remaining part of the stored charge is actively removed by a negative current through the diode.

During the initial period of this process known as reverse recovery, the negative current increases; with the development of a reverse voltage occurring only when the current attains a value of $I_{rrm}$, - the peak reverse recovery current. The developed model uses the parameters $I_{rrm}$, and $t_{rr}$ (the time taken for reverse recovery) as inputs.

The turn-off curves of the diode voltage and the current are fitted considering three distinct intervals of Fig. 3. In the interval $[t_{0 rej}, t_{1 rej}]$, $I_d$ is modeled as a linear slope, with $V_{f}=V_{dt}$ (forward voltage drop). In the period $[t_{1 rej}, t_{2 rej}]$, it is modeled by:

$$I_d(t) = -I_{1 rej} (t-t_{1 rej}) e^{-\alpha_{1 rej}(t-t_{1 rej})^2}$$

(1)

The unknown parameters in (1) are computed from datasheet information considering the defined points and the initial slope of the $I_d$ curve as:
Fig. 3. Idealized waveforms of diode turn-off transient

\[ k_D = I_{\text{rme}} e^{\frac{V_{dc}}{I_{\text{thr}}}} \left( \frac{dI_T}{dt} \right) \left( t_{i_{\text{on}}} \right) \]

\[ \alpha_{1(\text{on})} = \frac{1}{2} \left( k_D I_{\text{rme}} \right)^2 ; \quad I'_{1(\text{on})} = \sqrt{\frac{\alpha_{1(\text{on})}}{I_{\text{rme}}}} k_D e^{\frac{V_{dc}}{I_{\text{thr}}}} \]

(2)

In the region \( t > t_{2(\text{on})} \) the current and voltage are modeled by:

\[ I_d(t) = I_{\text{rme}} e^{-\alpha_{2(\text{on})} \left( I_{\text{rme}} \right)^2} \]

\[ V_d(t) = V_{1(\text{on})} e^{-\alpha_{2(\text{on})} \left( I_{\text{rme}} \right)^2} - V_d_0 \]

where \( V_{1(\text{on})} = V_{\text{off}} + V_d \). The condition that the reverse recovery current decays to 10% of \( I_{\text{rme}} \) after time \( t_r \) gives

\[ \alpha_{2(\text{on})} = \frac{\ln |10|}{t_{\text{rbb}}} = \frac{\ln |10|}{(1 - k_D)^2 t_{\text{r}}^2} \]

(5)

The energy lost can now be computed as:

\[ W_{\text{rec}} = \int_{t_{i_{\text{on}}}}^{t_{i_{\text{on}}}} \left[ V_d(t) I_d(t) dt + \int_{t_{i_{\text{on}}}}^{t_{i_{\text{on}}}} V_d(t) I_d(t) dt \right] \]

\[ \approx \frac{I_{\text{rme}}^2 V_d}{2 I_{\text{rme}}^2} + \frac{\pi}{2} \sqrt{2 V_d_0 - V_{1(\text{on})}} \]

(6)

Note that the particular forms of the functions chosen to represent the current and voltage variations are very important; these functions should not only follow the desired variations within the applicable region, but also facilitate the analytical integration of the voltage-current product to arrive at the formula for \( W_{\text{rec}} \); and be amenable to extraction of the values of parameters from the datasheet information.

2) IGBT Turn-on Loss Formula

Fig. 4 shows waveforms for the hard turn-on transient of an IGBT. In data sheets, the turn-on behaviour is characterized by the turn on delay time, \( t_{d\text{on}} \), the rise time, \( t_r \), and the turn-on energy, \( W_{\text{on}} \).

The turn-on gate pulse is applied at \( t_{d\text{on}} \) resulting in the gradual rise of the gate voltage \( V_{gg} \) (due to the input capacitance of the IGBT). After a time \( t_{d\text{on}} \), when \( V_{gg} \) reaches a threshold voltage \( V_{th} \), the collector current, \( I_c \), starts to rise almost linearly and the load current in the freewheeling diode (of the opposite leg) gradually transfers to the IGBT. During this rise, the device (collector-emitter) voltage \( V_{ce}(t) \) experiences a drop primarily due to parasitic inductance \( L_{pe} \).

The overshoot in \( I_c \) during \([t_{2\text{on}}] - [t_{4\text{on}}]\) is due to the reverse recovery current of freewheeling diode. The collector-emitter voltage \( V_{ce} \) begins to fall when the diode reverse recovery current reaches its peak value at \( t_{3\text{on}} \).

As with the case for the diode turnoff discussed above, applicable equations for the current and voltage waveforms can be derived for the various intervals, and the energy loss \( W_{\text{on}} \) is calculated as:

\[ W_{\text{on}} = \int_{t_{1\text{on}}}^{t_{1\text{on}}} V_{ce}(t) I_c(t) dt \]

\[ \approx \left( V_{c0} - V_{1(\text{on})} \right) I_{1(\text{on})} \left( 1.25 t_r + \frac{1}{\alpha_{1(\text{on})}} + \frac{1}{\alpha_{2(\text{on})}} \right) \]

\[ + V_{1(\text{on})} I_{1(\text{on})} + \frac{1}{\alpha_{1(\text{on})}} + \frac{1}{\alpha_{2(\text{on})}} \]

(7)

Appendix 1 provides an outline of the derivation and definitions for the parameters in (7).

3) IGBT Turn-off Loss Formula

The IGBT’s turn-off behaviour shown in Fig. 5 is characterized in data sheets by the turn-off delay time, \( t_{d\text{off}} \), fall time, \( t_f \), and turn-off energy, \( W_{\text{off}} \). The turn-off process starts following the application of negative gate voltage at time \( t_{d\text{off}} \). The input capacitance of the IGBT discharges gradually reducing gate-emitter voltage, \( V_{ge} \), but collector-emitter voltage, \( V_{ce} \), remains essentially unchanged until \( V_{ge} \) drops sufficiently to drive the IGBT out of saturation. This initial period is denoted by \( t_{d\text{off}} \) in the Fig. 5. Thereafter, the collector-emitter voltage rises rapidly. When \( V_{ce} \) reaches the forward blocking voltage \( V_{ceb} \) at \( t_{2\text{off}} \), the freewheeling diode become forward biased and starts to take over the load current.

![Diagram of IGBT turn-off process](image-url)

The IGBTs internal construction includes a MOSFET...
driving a bipolar transistor, and due to the mechanisms involved in these devices, the collector current \( I_c \) initially has a rapid fall; followed by a more gentle drop towards extinction at time \( t_{(off)} \). The rapid drop in current through the parasitic inductance produces an overshoot in the voltage \( V_{CE} \).

Again, using suitable expressions for the current and voltage over the various intervals (with details and parameters in Appendix 1); the following expression is obtained for the energy loss during turnoff \( W_{off} \):

\[
W_{off} = \int_{t_{(off)}}^{t_{(end)}} V_{CE}(t)I_c(t)dt \\
= \frac{1}{2} \left( \int_{t_{(off)}}^{t_{(end)}} V_{CE}(t)I_c(t)dt \right)^2 \\
+ \frac{1}{4\alpha_{1(0)}} \left( e^{-2\alpha_{1(0)}t} - e^{-4\alpha_{1(0)}t} \right) \\
+ \frac{1}{2\alpha_{2(0)}} \left( 1 - e^{-\frac{t}{\alpha_{2(0)}}} \right) \\
+ \frac{1}{2\alpha_{2(0)}} \left( 1 - e^{-\frac{t}{\alpha_{2(0)}}} \right) \\
+ \frac{1}{2\alpha_{2(0)}} \left( e^{-\frac{t}{\alpha_{2(0)}}} - e^{-\frac{t}{\alpha_{2(0)}}} \right) \\
+ \frac{1}{2\alpha_{2(0)}} \left( e^{-\frac{t}{\alpha_{2(0)}}} - e^{-\frac{t}{\alpha_{2(0)}}} \right) \\
+ \frac{1}{2\alpha_{2(0)}} \left( e^{-\frac{t}{\alpha_{2(0)}}} - e^{-\frac{t}{\alpha_{2(0)}}} \right)
\]

\( (8) \)

C. Validation of Switching Energy Models

The approach developed above was validated by comparison with published results from manufacturers’ data sheets as well as with a laboratory setup of the circuit in Fig. 2.

1) Comparison with Manufactures Data Sheets

The possibility of using the derived expression for switching energies with data sheet parameters was studied by computing switching energy verses collector current curves for several IGBTs. The parameters that are not available in the data sheets were estimated by adjusting their values to match with the switching energy at the rated current. Those parameter values are then used to predict the turn-on and turn-off losses at different collector currents. Two commercially available IGBTs (with anti-parallel diodes) from different manufacturers were considered, the SNR13H2500 from ABB, rated at 2.5 kV, 1300 A and the IXGK50N60BD1 from IXYS rated at 600 V, 65 A. The variation of calculated turn-on and turn-off energy losses (as in (7) and (8)) for these two devices are shown in Figs. 6 and 7 respectively; which also shows the loss curves supplied on the manufacturers’ data sheets.

As can be seen, the equations developed in this paper capture with reasonable accuracy, the variation of losses with current.

2) Experimental Confirmation

The test circuit as in Fig. 2 was set up in a laboratory. A 20 mH inductance was selected to ensure negligible current ripple; and the 4500 \( \mu \)F capacitor across the source was selected to ensure ripple free dc voltage. The on-state current in the device was adjusted by selecting the resistance \( R \) appropriately. The IGBT (the anti-parallel diode being included in the package) was rated at 600 V, 25 A (IRG4PC40KD). The voltage and current waveforms were measured and plotted for comparison with the piecewise fitting formulae derived in this paper (see Appendix 1) from which (7) and (8) are obtained. The plots for turn-on and turn-off are shown in Figs. 8 and 9 respectively and show good agreement.

The calculated energy loss from (7) and (8) was also compared with the measured energy loss; obtained by integrating the product of the measured voltage and current during switching.
The results, which were generated considering various combinations of two different voltages (150 V and 120 V) and currents (15 A, 20 A and 25 A) are shown in Table I. It can be seen that the maximum error is 21%, although in most cases the error is within 15%.

### Table I: Comparison of Measured and Calculated Power Losses for IRG4PC40KD IGBT

<table>
<thead>
<tr>
<th>$V_{ce}$ (V)</th>
<th>$I_{d}$ (A)</th>
<th>$W_{on}$ (mJ)</th>
<th>Error (%)</th>
<th>$W_{off}$ (mJ)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>15</td>
<td>0.193</td>
<td>21.9</td>
<td>0.183</td>
<td>10.9</td>
</tr>
<tr>
<td>150</td>
<td>20</td>
<td>0.274</td>
<td>13.9</td>
<td>0.289</td>
<td>10.0</td>
</tr>
<tr>
<td>150</td>
<td>25</td>
<td>0.353</td>
<td>18.1</td>
<td>0.394</td>
<td>21.3</td>
</tr>
<tr>
<td>120</td>
<td>15</td>
<td>0.155</td>
<td>11.6</td>
<td>0.112</td>
<td>11.6</td>
</tr>
<tr>
<td>120</td>
<td>20</td>
<td>0.221</td>
<td>9.5</td>
<td>0.183</td>
<td>12.0</td>
</tr>
<tr>
<td>120</td>
<td>25</td>
<td>0.310</td>
<td>4.8</td>
<td>0.289</td>
<td>11.1</td>
</tr>
</tbody>
</table>

### III. Modelling the Thermal Path

The models developed in this paper are intended for analyzing the thermal performance of the power electronic circuit when operating into an electrical network. The junction temperature of the device is an important parameter; an excessive value can damage the device. The mounting of the device and the heat-sink become important in determining the heat removal performance, and hence must be modeled accurately. The following section deals with this aspect.

#### A. Thermal Model of the IGBT

1) Thermal Equivalent Circuit

From a thermal point of view, the IGBT can be represented by a lumped parameter equivalent circuit as in Fig. 10. $P_{Lj}$ is the power loss in the device with $T_j$ and $T_a$ being the junction and case temperatures respectively. The nodal voltages correspond to intermediate temperatures within the device. $R_{th1}$ and $C_{th1}$ represent the thermal resistance and capacitance of various layers of the semiconductor device. The number of RC stages is usually determined by the number of materially different layers in the thermal path. It is often sufficient to model the heat sink as a single lumped thermal capacitance and resistance from the sink to the ambient temperature ($T_a$). If many devices are mounted on a common heat sink, the IGBT thermal equivalent circuit can be connected in tandem with the thermal equivalent of the heat sink as shown in Fig 10.

![Fig. 10. Equivalent thermal network of a semiconductor device and heat sink](image)

Fig. 10. Equivalent thermal network of a semiconductor device and heat sink

In Fig. 10, $T_a$ represents the case temperature of the $i^{th}$ device mounted on the heat sink and $R_{thi}$ are the corresponding thermal resistances between the case and heat sink.

State space equations of the above thermal equivalent circuit are set up and numerically solved to obtain the junction temperatures. To calculate the average loss power $P_{Lj}$ over a small measurement period, the total energy ($W_{cond}+W_{con}+W_{off}+W_{block}$) as described in section IIb is continuously calculated and divided by this measurement period. This measurement period is effectively the ’simulation time-step’ of the thermal equivalent circuit of Fig. 10.

2) Extraction of Model Parameters

Although, some manufacturers provide the values of $R_{th}$ and $C_{th}$ values in their device specification sheets, the information required to obtain thermal network parameters is commonly given in the form of a single-pulse junction to case transient thermal impedance ($Z_{th}$) curve shown in Fig. 11. This curve is first approximated by an analytical function having the form:

$$Z_{th}(t) = A_0 + \sum_{i=1}^{n} A_i e^{-a_i t}$$  \hspace{1cm} (9)

where $A_0$...$A_n$ and $a_1$...$a_n$ are constants to be found through an appropriate curve fitting technique. The $R_{th}$ and $C_{th}$ values are then obtained from the $A_i$ and $a_i$ as shown in Appendix 2. The derived $A_i$ and $a_i$ constants and the corresponding $R_{th}$ and $C_{th}$ for IXER 35N120D1 IGBT/Diode module are shown in Table II. As can be seen from Fig. 11, the $Z_{th}$ curves obtained from the fitted thermal models (with 2 stages) show good agreement with the corresponding data sheet curves.

![Fig. 11. Transient thermal impedance curves of IXER 35N120D1 [14]](image)

### Table II: Thermal Path Model Parameters of IGBT

<table>
<thead>
<tr>
<th>$A_0$ (W/K)</th>
<th>$A_1$ (W/K)</th>
<th>$A_2$ (W/K)</th>
<th>$a_1$ (s$^{-1}$)</th>
<th>$a_2$ (s$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.600</td>
<td>1.300</td>
<td>-0.499</td>
<td>-1.099</td>
<td>0.212</td>
</tr>
<tr>
<td>0.238</td>
<td>0.523</td>
<td>0.095</td>
<td>0.064</td>
<td>0.133</td>
</tr>
</tbody>
</table>

**IGBT**

<table>
<thead>
<tr>
<th>$R_{th}$ (K/W)</th>
<th>$C_{th}$ (J/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.238</td>
<td>0.523</td>
</tr>
</tbody>
</table>

**Diode**

<table>
<thead>
<tr>
<th>$R_{th}$ (K/W)</th>
<th>$C_{th}$ (J/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.095</td>
<td>0.064</td>
</tr>
<tr>
<td>0.240</td>
<td>0.133</td>
</tr>
</tbody>
</table>
IV. APPLICATIONS

A. The composite electro-thermal model

The power loss estimation model and the thermal models of the device and heat sink were implemented in the PSCAD/EMTDC program. As discussed in Section IIa and shown in Fig. 1, the existing semiconductor switch model was modified to include the loss calculations of section IIb. The loss model calculates and outputs power dissipation (including conduction, blocking and switching losses) in the switching device during a simulation time step. The power dissipation is input to the thermal model discussed in section III, which in turn calculates the junction (and other) temperatures. The junction temperature is fed back to the device power loss calculation in the following time-step so that the temperature dependent parameters ($V_{ces}$ and switching times) can be updated.

B. Example: VSC with Hysteresis Current Control

The methods developed above were used in the loss and thermal evaluation of the voltage source converter (VSC) of Fig. 12. The converter is controlled using hysteresis current control, which maintains the current in any phase within a specified tolerance band around the reference current setting. This is achieved by switching on the IGBT in the upper bridge arm when the current is below the lower tolerance level; and switching on the lower IGBT when the current is larger than the upper tolerance level. Unlike conventional sinusoidal PWM, the switching events and their frequency are highly load dependent and so an a-priori estimation of switching losses is difficult.

The inverter uses using six IXER 35N120D1 IGBT/Diode modules and parameters required for the models were obtained from its datasheet [14]. Fig. 13 shows the reference current of Phase-A and the actual load currents in all three phases. The relatively large hysteris band seen in the load current ($\Delta I=10A$) was deliberately set in order to clearly observe the waveforms.

Fig. 14 shows the total energy loss as a function of time. The conduction loss is proportional to the magnitude of the current. The spikes at the beginning and end of conduction periods correspond to turn-on and turn-off losses respectively. In the diode, reverse recovery energy losses appear as spikes at the end of conduction periods.

The variations of the junction temperatures of the IGBT ($T_j$) and diode ($D_1$), and the module case temperature for an ambient temperature of 25°C are shown in Fig. 15. The depicted waveforms are for a transient state in which the temperatures are still increasing enroute to their steady state values (average 87°C for the IGBT junction temperature) which are attained in approximately 10 s. Peaks of the ripples appearing in the junction temperatures coincide with the respective device current peaks, and their influence on temperatures is smoothed out due to thermal capacitance.

Table IV shows numerical values of the losses for two different hysteresis band widths. As can be seen, the switching losses increase with a smaller hysteresis band (i.e. higher operating frequency), with the conduction losses remaining fairly constant. The breakdown of the losses into various components is also shown in the table.

<table>
<thead>
<tr>
<th>TABLE IV: LOSS BREAKDOWN AND VARIATION WITH HYSTERESIS BANDWIDTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of loss per device</td>
</tr>
<tr>
<td>(60 Hz load current)</td>
</tr>
</tbody>
</table>
V. CONCLUSIONS

This paper introduces modifications to the existing models of semiconductor switches in electromagnetic transients programs to account for losses. The approach, which is based on interpolating analytically integrable equations to the voltage and currents during the switching event, is reasonably accurate without requiring excessively small time-steps. All necessary parameters of the models can be estimated from manufacturer’s data sheets or more accurately determined from test waveforms where available.

The accuracy of the loss calculation formulae were confirmed by comparison with a simple laboratory setup.

A method for calculation of temperature increase in the semiconductor devices and the procedure of extracting the required parameters from transient thermal impedance curves was also presented.

Although the devices considered here were the IGBT and the diode, the procedure is easily generalizable to most other power electronic systems.

The applicability of the procedure was demonstrated by considering the losses of a hysteresis controlled current reference PWM inverter. The procedure yielded the different components of the losses, as well as the dynamics of the variations of junction temperatures. The example clearly demonstrates that the developed approach would be useful in the design of thermal management systems for power electronic converters embedded in a large electrical network.

VI. APPENDIX 1

A. Turn-on Transient

The turn-on transient period is divided into three sections, \([t_{1(on)} - t_{2(on)}], [t_{2(on)} - t_{3(on)}] \) and \([t_{3(on)} - t_{4(on)}] \) (see Fig. 4) to derive the voltage and the current curves with:

\[
I_{1(on)} = I_{0(on)} + I_{d(on)} - \frac{1}{8} r_f, \quad I_{2(on)} = I_{1(on)} + \frac{10}{8} r_f, \quad I_{3(on)} = I_{2(on)} + k_D r_f, \quad I_{4(on)} = I_{2(on)} + I_{rr} + I_{tail}
\]

During \([t_{1(on)} - t_{2(on)}], \) \(I_c \) and \(V_{ce} \) are defined as:

\[
I_c(t) = I_{1(on)} \left[1 - e^{-\lambda_{cek}(t-t_{1(on)})}\right]
\]

\[
V_{ce}(t) = V_{ce}(0) \left[1 - e^{-\lambda_{cek}(t-t_{1(on)})}\right]
\]

Considering the almost linear rise of current, it is assumed that \(I_{1(on)} \approx 100 I_{0} \) where \(I_{0} \) is the on state current. Then

\[
\lambda_{cek}(on) = \frac{1}{1.25r_f} \ln \left[\frac{1}{0.99}\right]
\]

An approximate value for \(V_{1(on)} \) can be obtained considering the average \(dI_c/dt \) across the parasitic inductance \(L_p \).

\[
V_{1(on)} = \frac{g_{mD}}{r_c} I_p
\]

Factor \(\lambda_{cek}(on) \) is obtained assuming 90% decay of \(V_{1(on)} \) during the considered period:

\[
\lambda_{cek}(on) = \frac{1}{1.25r_f} \ln \left|10\right|
\]

During \([t_{2(on)} - t_{3(on)}], \) the collector current is the sum of load current and the reverse recovery current given in (1) while \(V_{ce} \) remains at plate Voltage \(V_{ce} \) defined below:

\[
I_c(t) = I_{0(on)} + I_{rr}(t-t_{2(on)}) e^{-\alpha_{cek}(t-t_{2(on)})^2}
\]

\[
V_{ce} = V_{ce}(0) - L_p \frac{0.8}{r_c} t_f
\]

After \(t_{3(on)}, \) the reverse recovery current gradually decays according to (3) while \(V_{ce} \) falls towards its saturation value \(V_{ces} \). It is assumed that \(V_{ce} \) consist of two components decaying at different rates:

\[
I_c(t) = I_{0(on)} + I_{rm} e^{-\alpha_{cek}(t-t_{3(on)})^2}
\]

\[
V_{ce} = V_{2(on)} e^{-\alpha_{cek}(t-t_{3(on)})^2} + V_{3(on)} e^{-\alpha_{cek}(t-t_{3(on)})^2}
\]

The coefficient \(V_{3(on)} \) of the slow decaying component of \(V_{ce} \) is equal to the tail voltage \(V_{tail} \) shown in Fig. 4, and appears approximately proportional to plateau voltage \(V_{cep} \). Thus the factor, \(k_{\text{cep}} \) [0-1], which characterizes the tail size is defined such that:

\[
V_{tail} = k_{\text{cep}} V_{cep}
\]

Then the magnitude of the fast decaying component (which decays at the same rate as diode reverse recovery current) is:

\[
V_{2(on)} = (1-k_{cep}) V_{cep}
\]

The fact that the tail voltage drops to \(V_{ces} \) at \(t_{4(on)} \) gives:

\[
\lambda_{cek}(on) = \frac{1}{(1-k_D) \ln \left[\frac{k_{cep} V_{cep}}{V_{ces}}\right]} V_{ces}
\]

B. Turn-off Transient

Expressions for the current and the voltage during the turn-off are defined considering two intervals, \([t_{0(off)} - t_{2(off)}] \) and \([t_{2(off)} - t_{3(off)}] \) (see Fig. 5) where:

\[
t_{2(off)} = t_{0(off)} + I_{rr} \frac{1}{8} t_f
\]

\[
t_{3(off)} = t_{0(off)} + \frac{1}{8} t_f + t_{tail}
\]

During \([t_{0(off)} - t_{2(off)]}, \) \(I_c \) remains at \(I_{0} \), while \(V_{ce} \) rises starting from its saturation value according to:

\[
V_{ce}(t) = V_{ces}(0) + \frac{1}{8} t_f V_{ces} e^{\lambda_{cek}(t-t_{0(off)})}
\]

where

\[
I_{1(off)} = I_{0} + k_{vd} \frac{I_{d(off)} - \frac{1}{8} t_f}{V_{ces}}
\]

\[
V’ = -\frac{0.1 V_{ces} - V_{ces}}{k_{vd} (I_{d(off)} - \frac{1}{8} t_f)}
\]

\[
\lambda_{ked}(off) = \ln \left[\frac{V_{ces} - V_{ces}(off)}{V_{ces}}\right] (1-k_{vd}) \frac{I_{d(off)} - \frac{1}{8} t_f}{t_f}
\]

\[
k_{vd} \approx I_{d(off)}/I_{d(off)}
\]

During \([t_{2(off)} - t_{3(off)]}, \) the \(I_c \) falls according to
A. Extraction of Thermal Model Parameters

The values of $R_{th}$ and $C_{th}$ values are calculated from the coefficients of (9) as shown below. Generally, two exponential terms (i.e. $n = 2$ in (9)) can sufficiently accurately approximate the $Z_{th}$ curve. For $n = 2$, the values of $R_{th}$ and $C_{th}$ are:

$$R_{th} = \frac{q^2}{(q - p)s}, \quad R_{th2} = p - q^2/(q - ps)$$

$$C_{th} = s/q, \quad C_{th2} = (q - ps)^2/q(pqr - p^2s - b^2)$$

where,

$$p = A_0, \quad q = A_0\ln\left(\frac{1}{a_1} + \frac{1}{a_2}\right) + A_1\ln\left(\frac{1}{a_1}\right) + A_2\ln\left(\frac{1}{a_2}\right)$$

$$r = \frac{1}{a_1} + \frac{1}{a_2}, \quad s = \frac{1}{a_1a_2}$$

VIII. REFERENCES


IX. BIographies

A.D. Rajapakse (M’99) obtained his B.Sc. (Eng) degree from the University of Moratuwa, Sri Lanka in 1990, M.Eng. degree from the Asian Institute of Technology, Thailand in 1993 and Ph.D. degree from the University of Tokyo in 1998. He is currently a Visiting Professor at the University of Manitoba. Dr. Rajapakse’s research interests include transient simulation of power and power electronic systems, application of fuzzy logic, neural networks and genetic algorithms in modeling and control of dynamic systems, renewable energy systems and energy conservation.

A. M. Gole (M’82) obtained the B.Tech. (EE) degree from IIT Bombay, India in 1978 and the Ph.D. degree from the University of Manitoba, Canada in 1982. He is currently a Professor of Electrical and Computer Engineering at the University of Manitoba. Dr. Gole’s research interests include the utility applications of power electronics and power systems transient simulation. As an original member of the design team, he has made important contributions to the PSCAD/EMTDC simulation program. Dr. Gole is active on several working groups of CIGRE and IEEE and is a Registered Professional Engineer in the Province of Manitoba.

P. L. Wilson (M’00) graduated from the University of Manitoba in 1987 in Electrical Engineering where he joined Manitoba Hydro. In his professional career he has held several positions including distribution engineer, design engineer, project manager, and department manager.
engineer, protection design engineer, maintenance engineer, and project manager. Paul became the Managing Director of the Manitoba HVDC Research Centre, November 1999. Along with his general duties, Paul is an active member of the IEEE and CIGRE, and practicing member of the APEGM. Paul Wilson lives in Winnipeg, Manitoba with his spouse Colleen and two children.