

# Improving conducted EMI forecasting with accurate layout modeling

M. Lionet\*, R. Prades\*, X. Brunotte\*, Y. Le Floch\*, E. Clavel\*\*, J.L. Schanen\*\*, J.M. Guichon\*\*

\*CEDRAT, 15 chemin de Malacher - F- 38246 Meylan Cedex, software@cedrat.com

\*\* G2ELab – Grenoble Electrical Engineering Laboratory, ENSIEG - BP 46 - F- 38402 St-Martin-d'Hères Cedex, jean-luc.schanen@g2elab.inpg.fr

**Abstract** - This paper describes how layout modeling of power module has been used to forecast conducted electromagnetic interferences (EMI) of an integrated converter. PEEC method has been used to account for inductive parasitic of printed circuit board (PCB) bus bars, Direct Bonded Copper (DBC) substrate, wire bonds and heat spreader. After validation in simple example of three-phase inverter, cabling model has been implemented in circuit simulation to forecast conducted EMI.

## I. INTRODUCTION

As the use of power electronic devices is getting more and more important, improving their efficiency and reliability becomes a major issue. The level of electromagnetic interference (EMI) is a determining factor for the electrical performance of a system and, regarding these aspects, the geometrical structure plays a decisive role. Therefore, predicting with a satisfying accuracy the electromagnetic compatibility (EMC) requires precise models of components and electrical interconnections. The non ideal behavior of the cabling can be modeled thanks to Partial Element Equivalent Circuit (PEEC) method. This paper presents a study carried out on a power module with a focus on the modeling of the cabling using InCa3D software [1]. The model of the module's internal connections and busbars will be presented in section II. To validate the PEEC model, a comparative study between several modeling results and measurements will be done in section III. Knowledge of the electrical behavior of the cabling thanks to a reduced impedance matrix allows EMC analysis to be performed. By integrating the cabling model into a circuit simulator, the conducted EMI can be computed as shown in part IV.

## II. CONNECTIONS MODELING OF A POWER MODULE

### Modeling method

The internal layout of a power module (Direct Bonded Copper - DBC, wire bonds, PCB for

gate drive ...) builds up a very complex 3D geometry. To model the electrical behavior of the power module interconnections, global and local phenomenon have to be considered with the same resolution. Even if finite element methods appear to be well adapted to determine local physical features, the necessity to take into account the whole structure to determine global values like inductances rules out this method. PEEC method has already shown its great efficiency to compute parasitic inductances for these kinds of complex systems [2]. Implemented in the InCa3D software, this PEEC approach is based on analytical formula to compute stray inductances and couplings [3]. Provided that there is no magnetic material and that the current density is uniform, each conductor is modeled as described on Fig. 1 by its resistive (R) and inductive (L) contribution in addition to the mutual coupling among conductors (M).

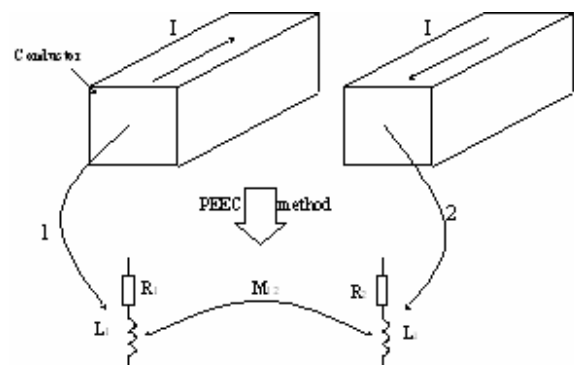


Fig. 1. PEEC modeling principle

To satisfy the second condition mentioned previously a meshing of the conductors, where each element is represented by an RLM equivalent circuit, is done. Applied to the complete system modeled, the PEEC approach provides an electrical equivalent circuit of the analyzed layout as presented in Fig. 2.

Obviously the size of the circuit obtained and the resulting impedance matrix depend on the mesh number. Attention has thus to be paid to have a sufficient number of elements to model correctly the electrical phenomena but without exceeding the calculator memory capacities. The investigation undertaken for this study to determine the appropriate meshing of each conductor will not be detailed in this paper. [4]

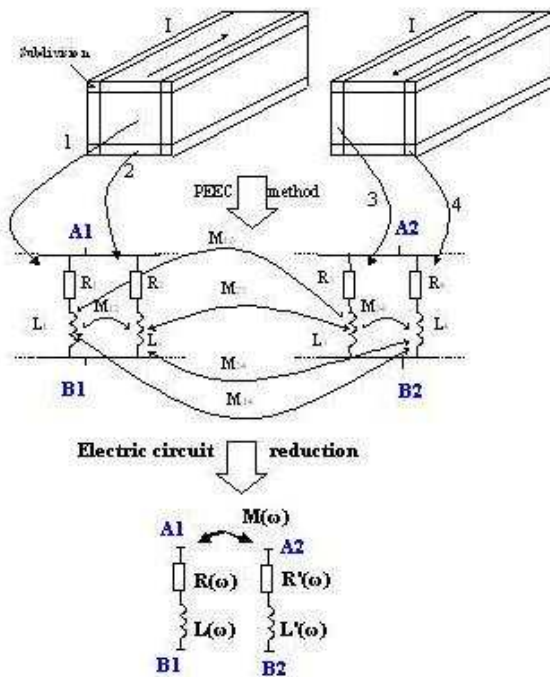


Fig.2. PEEC modeling with meshing and model reduction principle

Considering the impedance matrix obtained with PEEC method, the interest lies in the fact that it can be used by circuit simulators for transient analysis. Once an appropriate mesh has been set, the equivalent resistive and inductive contributions i.e.  $[R]$  and  $[M]$  matrix are computed. See (1) where  $n$  is the number of partial elements. The advantage of the PEEC method is that these matrixes are computed only once as they exclusively depend on the geometry. (2) explains how the impedance of the system is obtained by introducing the frequency.

$$[R] = \begin{bmatrix} R_1 \\ \vdots \\ R_i \\ \vdots \\ R_n \end{bmatrix} \quad [M] = \begin{bmatrix} L_1 & & & \\ & \ddots & & \\ & & L_i & M_{ij} \\ & & M_{ij} & \ddots \\ & & & & L_n \end{bmatrix} \quad (1)$$

$$[Z] = [R] + j\omega[M] \quad (2)$$

As  $[Z]$  is a full  $n \times n$  matrix, its size is prohibitive for subsequent circuit simulation. The impedance matrix is thus reduced to be used in a circuit simulator where all the components of the inverter (passives, sources, semi conductors...) are added. To achieve the system reduction, the input/output points are identified and thanks to circuit equations solving, a reduced impedance matrix corresponding to a vision of the geometry seen from these connecting points is obtained. This leads to a smaller equivalent circuit (see Fig. 2.), in which all values depend on the frequency used for the model reduction. The reduced model obtained can be exported to the simulator [5].

### Technological aspects of the power module

This studied power electronic module (600V – 75A nominal current) is a complete three phase inverter including 6 control pins and multiple pins for power connections. It is designed for AC motor control, and its maximum switching frequency is 20 kHz.

The three phase inverter contains 12 semiconductor components (6 IGBT and 6 free wheeling diodes) to perform 6 switch functions. Fig. 3. represents the electrical diagram of the inverter with these semiconductors and includes the input and output connections as well as an input capacitance that minimizes the voltage undulation and acts as a power supply.

To get the equivalent circuit of the power module studied, all connections of the system that play an electrical role have to be modeled within the InCa3D geometry descriptor. So, geometry of pins, wire bonds, DBC substrates, as well as the heat spreader are described. This heat spreader does not have any electrical connection with the rest of the module, but it acts on it like a ground plane. It has therefore an influence on the self and mutual inductances of the other conductors situated close to it.

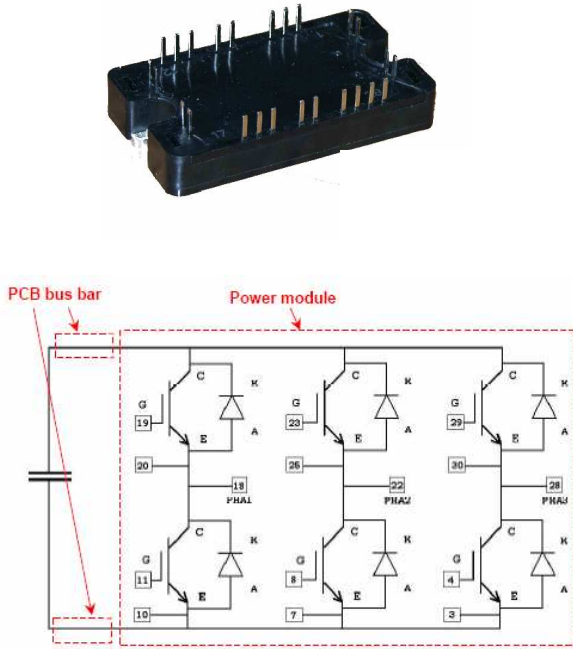


Fig. 3. Schematic diagram of the power module (APT). Top: picture of the power module

In addition to the internal connections of the power module described before the input PCB busbars have been represented within the InCa3D model that is presented in Fig. 4.

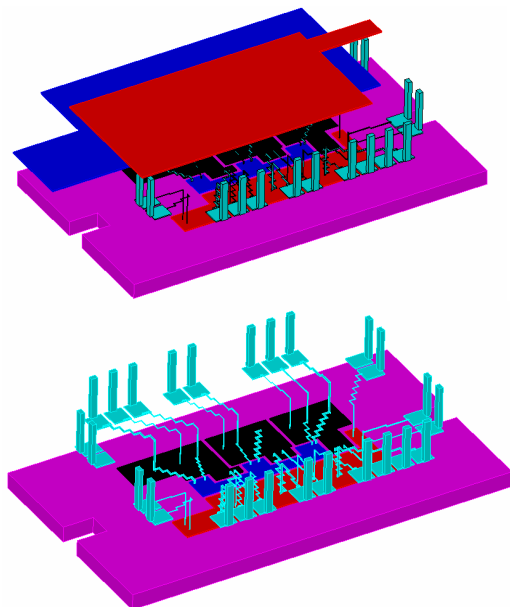


Fig. 4. View of the InCa3D model of the power module. Top: with PCB bus bars; Bottom: without PCB bus bars

### III. MODEL VALIDATION

An export from InCa3D of the reduced impedance matrix to simulation tools like Saber or Portunus [6] makes it possible to include the cabling model within circuit simulation. This enables transient analysis of the complete circuit. In addition, inductance calculation can be performed directly in InCa3D software. The switching loop inductance is the comparison criteria selected for this study.

In order to check the accuracy of the PEEC model, a series of tests has been made. The aim was to compare inductance of the loop presented in Fig. 5.

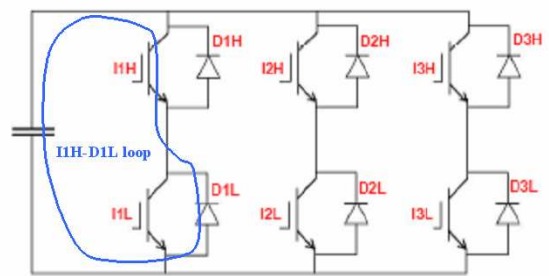


Fig. 5. I1H-D1L loop on the power module electric diagram

This value has been obtained either by measurements, direct computing in InCa3D or by circuit simulation including the PEEC model. The last method consists in modeling with a circuit simulator the inverter thanks to discrete component and to add the InCa3D cabling model in order to account for the non ideal behavior of the connections. A transient analysis permits to obtain the over voltage that appears during switching phases as well as the current waveform and thus to calculate the inductance value.

Table 1 presents the results obtained on the power module modeled without the input busbars.

	Measurement	InCa3D	Saber with InCa3D model	Difference InCa3D/ Measurement	Difference InCa3D/ Saber
Inductance for I1H-D1L loop	75.00 nH	71.35 nH	72.60 nH	5.11%	1.75%

Table 1. Measurement and simulation values for I1H-D1L loop inductance – without input PCB busbars



The value of the capacitance may be worked out either by measurements as has been done in this study, either by calculation through simple analytic formulae or by finite element analysis.

It has to be noticed that the capacitive model used here is quite simple and may be improved. Besides, the load used for this simulation is not representative of the reality as a simple R-L load is modeled. More accurate model could have been used as done in [8]. However, the aim of this study is not to present much accurate results on the conducted EMI but to show how this kind of investigation is possible.

Besides, to compute the conducted EMI, the inverter is connected to power supply through a Line Impedance Stabilisation Network (LISN). Fig. 6 presents an equivalent diagram of the three-phase inverter, LISN and load, where all interconnections of the power module are summarized into a single macro-component.

The FFT of LISN voltage provides conducted EMI simulation and the results of the study undertaken with the power module are presented in Fig. 7.

Combined to more precise load and power module capacitive models, a sensibility study could also be achieved with this modeling method as has been done in [9]. The approach of associating precise cabling models, components

and load into a circuit simulation is very interesting to evaluate the impact of integration technologies modifications on EMC emissions. One could imagine using the methodology presented in this paper to compare the EMI spectrum modeled to international EMC standards. Integrating these considerations early in the design process could have significant impact on the developing cost of new products by reducing the number of prototypes.

## V. CONCLUSION

Simulations on conducted EMI of a three-phase inverter have been carried out. The modeling with PEEC method of a power module interconnections to account for inductive stray elements has been presented. The inductive behavioral model of connections obtained with InCa3D has been successfully validated. Thanks to the automatic coupling this model can be exported to circuit simulator. The electric circuit is completed by a capacitive model and by the other components which allows the computing of the current and voltage waveforms. That way, the power module's EMI spectrum can be forecasted and the EMC performance estimated.

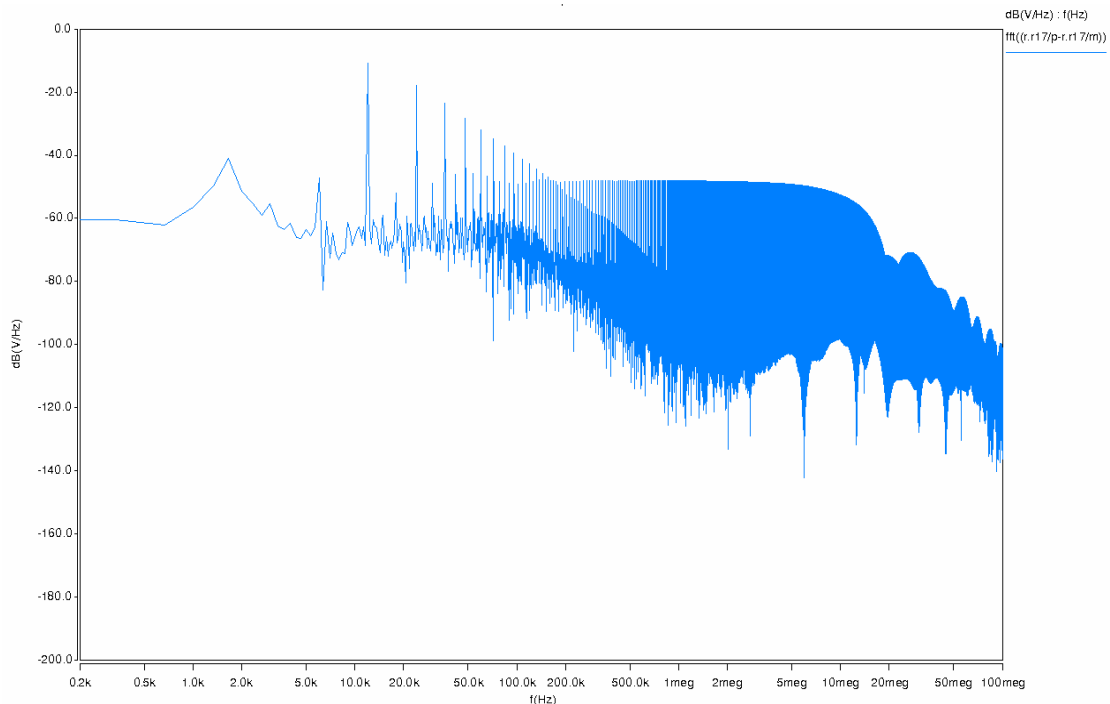


Fig. 7. LISN voltage spectrum obtained with circuit simulation

## ACKNOWLEDGEMENT

The authors wish to thank Hispano-Suiza company for providing the power module studied and the measurement results used in this study.

## REFERENCES

- [1] CEDRAT, *InCa3D user's guide*, www.cedrat.com, 2006
- [2] C. Martin, J.L. Schanen, F. Verdiere, R. Pasterczyk, *Modélisation de l'ensemble de la connectique d'un onduleur triphasé de 200kVA*, EPF'02, DEC 2002
- [3] A.E. Ruehli, *Inductance Calculation in a complex Integrated Circuit Environment*, IBM Journal of Res. and Dev., Sept. 1972
- [4] J-P. Gonnet, E. Clavel, V. Mazauric, J. Roudet, *PEEC Method dedicated to the design of electrical systems*, PIERS04, Mars 2004
- [5] J-L.Schanen, C.Martin, D.Frey, R.Pasterczyk, *Impedance criterion for power modules comparison*, IEEE trans on Power Electronics, Jan 2006, vol. 21, no. 1, pp 18-26
- [6] CEDRAT, *Portunus<sup>®</sup> user's guide*, www.cedrat.com, 2007
- [7] J. Robert, *Caractérisation d'un onduleur avec IGBT trench + field stop et diode SiC*, ENSEM, 2006
- [8] B. Revol, J. Roudet, J.L. Schanen, P.Loizelet, *EMI study of a three phase inverter-Fed Motor Drives*, IEEE IAS 04, Oct. 2004
- [9] P. Musznicki, J.L. Schanen, B. Allard, P.J Chrzan, *Accurate Modeling of Layout Parasitic to Forecast EMI Emitted from a DC-DC Converter*, PESC'04, June 2004